

WHAT IS CLAIMED IS:

1. A semiconductor device comprising a first
semiconductor chip consisting of at least either a circuit
5 against static damage or a passive component.

2. The semiconductor device according to claim 1,
wherein
said passive component includes at least one of a
10 resistor, a capacitor and a reactor.

3. The semiconductor device according to claim 1,
wherein
said first semiconductor chip consists of only said
15 passive component.

4. The semiconductor device according to claim 3,
wherein
said passive component includes all of a resistor, a
20 capacitor and a reactor.

5. The semiconductor device according to claim 1,
further comprising a second semiconductor chip and a third
semiconductor chip installed on a support substrate,
25 wherein

said second semiconductor chip and said third semiconductor chip are connected with each other through said first semiconductor chip.

5 6. The semiconductor device according to claim 5, wherein

10 said second semiconductor chip and said third semiconductor chip include no circuits against static damage.

10 7. The semiconductor device according to claim 5, wherein

15 said second semiconductor chip is a DRAM chip, and said third semiconductor chip is a logic chip.

15 8. A semiconductor device comprising:

 a plurality of semiconductor chips installed on a support substrate; and

20 a wire connecting said plurality of semiconductor chips with each other and having a passive component function.

 9. The semiconductor device according to claim 8, wherein

25 said wire having a passive component function has a

length greater than that for linearly connecting terminals of said plurality of semiconductor chips with each other thereby forming a resistive element.

5 10. The semiconductor device according to claim 8, further comprising a dummy wire fixed to a prescribed potential and arranged to be opposed to said wire at a prescribed interval, wherein

10 said wire is combined with said dummy wire to form a capacitor.

11. The semiconductor device according to claim 8, wherein

15 said wire is formed either in a single layer or in two layers.

12. A semiconductor device having a plurality of semiconductor chips installed on a support substrate, wherein

20 at least one of said semiconductor chips includes:

 a first input/output terminal, employed for testing an independent operating state of said semiconductor chip, having a first circuit against static damage,

25 a second input/output terminal, employed for connecting said semiconductor chip to said support

substrate, having a second circuit against static damage,
and

a third input/output terminal other than said first
input/output terminal and said second input/output

5 terminal, and

said plurality of semiconductor chips are connected
with each other through said third input/output terminal.

10 13. The semiconductor device according to claim 12,
wherein

said third input/output terminal includes no circuit
against static damage.

15 14. The semiconductor device according to claim 13,
wherein

said third input/output terminal includes only a
resistor.

20 15. The semiconductor device according to claim 12,
wherein

said third input/output terminal includes a third
circuit against static damage, and

a transistor forming said third circuit against
static damage is smaller than transistors forming said
25 first and second circuits against static damage.

16. The semiconductor device according to claim 15,
wherein

the gate width of said transistor forming said third
5 circuit against static damage is smaller than the gate
width of said transistors forming said first and second
circuits against static damage.

17. The semiconductor device according to claim 12,
10 wherein

said third input/output terminal includes a third
circuit against static damage,

said third circuit against static damage is formed by
a diode, and

15 said first and second circuits against static damage
are formed by transistors.

18. The semiconductor device according to claim 12,
wherein

20 said plurality of semiconductor chips include a DRAM
chip and a logic chip.

19. A semiconductor device having a plurality of
semiconductor chips installed on a support substrate,
25 wherein

at least one of said semiconductor chips includes:
a first input/output terminal and a second
input/output terminal,

a first circuit against static damage connected to
5 said first input/output terminal, and

switching means connected between said first
input/output terminal and said first circuit against
static damage and on-off controlled by said second
input/output terminal.

10

20. The semiconductor device according to claim 19,
wherein

said switching means is set to an ON state by
applying no voltage to said second input/output terminal
15 during a step of fabricating said semiconductor chips and
set to an OFF state by applying a prescribed voltage to
said second input/output terminal after completion of a
chip connection step following fabrication of said
semiconductor chips.

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21. The semiconductor device according to claim 19,
wherein

said first circuit against static damage includes
first and second transistors, and

25 said switching means includes:

a third transistor connected between said first transistor and said first input/output terminal to enter an ON state when no voltage is applied to said second input/output terminal and enter an OFF state when said
5 prescribed voltage is applied to said second input/output terminal, and

a fourth transistor connected between said second transistor and said first input/output terminal to enter an ON state when no voltage is applied to said second
10 input/output terminal and enter an OFF state when said prescribed voltage is applied to said second input/output terminal.

22. The semiconductor device according to claim 19,
15 wherein

a second circuit against static damage is connected to said second input/output terminal.